NONLINEAR ANALYSIS OF A MICROWAVE SYNTHESIZER BASED ON A SAMPLING-PHASE DETECTOR

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***Abstract* — A microwave synthesizer operating at 6.52 GHz and based on a sampling-phase detector has been designed and simulated. The employment of nonlinear-analysis tools has enabled an in-depth study of the system dynamics. Hold-in and lock-in bands are determined in a direct and accurate way through the use of the Poincaré-map technique. The nonlinear analysis has also made possible the a-priori determination of the loop-filter and VCO characteristics for a good performance in terms of phase noise and loop dynamics.**

I. INTRODUCTION

A microwave synthesizer at 6.52 GHz, to operate in a downconverter for a satellite-communication system, has been designed. Due to the restricted phase-noise specifications, a low-order frequency divider is employed in the phase-locked loop. This requires a high-frequency reference signal, which is obtained using a sample-phase detector (SPD). This detector is constituted of a step-recovery diode and a Schottky-diode mixer [1]. When excited with a sinusoidal voltage, at the frequency ω_x, the step recovery diode ideally provides a pulsed output current. This enables very high-order multiplication of the input-signal frequency. Appropriate output filtering in order to select the desired harmonic frequency $K_L \omega_x$ and avoid spurious frequency components. A very narrow bandwidth in the filter, although positive for the phase-noise behavior, leads to a severe reduction of the phase-locking bands. An acquisition-aid circuit is usually required.

An in-depth nonlinear analysis of the SPD-based phase-locked loop has been carried out here. This has enabled a better understanding of the complex system dynamics and the determination of the lock-in and hold-in bands about the desired frequency component. These bands are inherent to the phase-locked system. Even when using an acquisition-aid circuit, their knowledge allows helpful estimations for the necessary VCO sensitivity and for the amplitude of the control signal.

As in [2], the nonlinear analysis is based on the use of realistic models for the loop elements. Here the Poincaré-map technique is employed for the first time to determine the phase-locking bands in an accurate and direct way. This study, together with an estimation of output phase-noise for different values of the loop-filter bandwidth, has enabled an optimized performance of the microwave synthesizer.

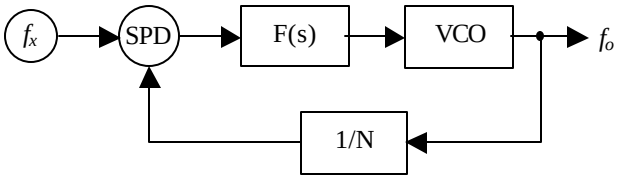


Fig. 1 Schematic of the microwave synthesizer based on a sampling-phase detector SPD.

II. DESIGN OF THE MICROWAVE SYNTHESIZER

A microwave synthesizer with the general block diagram of Fig. 1 is initially considered. The desired output frequency is 6.52 GHz with output phase noise –73 dBc/Hz at 10 KHz. The phase noise is due to three major contributions, coming from the reference oscillator, the VCO and the frequency divider. The use of a low-noise divider allows neglecting its contribution. In a linearized analysis, about a constant phase solution, the output-phase noise is given by [3]:

$$L(w) = 20\log\left|\frac{jwN}{jwN + G\,F(w)}\right| + L_{VCO}(w) + 20\log\left|\frac{N\,G\,F(w)}{jwN + G\,F(w)}\right| + L_R(w) \quad (1)$$

In the above expression L_R, L_{VCO} and L are respectively the reference, VCO and output phase noise, in dBc/Hz, N is the frequency division order, G, the total loop gain and F(ω), the loop-filter transfer function. From inspection of (1), the reduction of the division order N decreases L(ω), close to the oscillator carrier. Here an order N = 4 has been chosen, which would imply a reference frequency f_r =1.63 GHz. Such a high value is obtained through frequency multiplication, using a SPD. The pulsed output current from the step-recovery diode provides harmonic components of very high order. Using a crystal oscillator of frequency f_x = 10 MHz, the harmonic component K_L = 163 must be selected. The elimination of the neighboring harmonic frequencies is demanding from the filtering point of view.

The noise at the reference input L_R is due to the crystal oscillator and SPD block. Taking into account the multiplication factor K_L, it can be approximated by $L_R(\omega) = L_X(\omega) + L_{SPD} + 20 \log (K_L)$, with $L_X(\omega)$ being the crystal-oscillator phase noise.

The convenience of choosing a function $F(\omega)$ with a pole located at the origin is evidenced in (1). Initially a two-pole loop filter has been considered, with the transfer function:

$$F(s) = \frac{(\tau_1 s + 1)}{\tau_2 s\ (\tau_3 s + 1)} \qquad (2)$$

From the insertion of this filter in the schematic of Fig. 1, a type-II third order PLL is obtained. The parameters τ_1, τ_2 and τ_3 are chosen so that the curve (1) is below the phase-noise specifications. The resulting phase margin is 70º and the cut-off frequency 4.2 MHz. However this linear estimation does not guarantee enough filtering of spurious frequencies.

The difference-frequency term at the SPD output is $f_{IF} = f_o - K_L f_x$, with f_o being the VCO output frequency. The frequency separation between the pulse harmonic components is f_x, so the closest spurious frequencies are $f_{IF} + f_x$ and $f_{IF} - f_x$. Thus the filter must provide enough rejection at f_x and additional poles might be required to eliminate spurious frequencies. As mentioned above, excessive filtering may lead to very slow dynamics and severe reduction of the lock-in bands.

III. Nonlinear Analysis Of The Microwave Synthesizer

The nonlinear analysis should provide a better understanding of the actual system behavior and enable the prediction of lock-in bands and spurious content. Note that the analysis of spurious frequencies is crucial in the case of pulse input.

A realistic nonlinear characteristic for the VCO is taken in to account, including saturation effects, which, as in [2], are modeled through an hyperbolic tangent. The mixer is simulated as a signal multiplier. In the filter, the actual circuit elements are considered.

A. Steady-state analysis

The nonlinear equation ruling the VCO output frequency is [2]:

$$f_o^v = w_o + M_1\ \mathrm{tgh}\left[M_2\ u_2(t)\right] \qquad (3)$$

with $u_2(t)$ being the loop-filter output signal and M_1 and M_2, two different fitting constants. The result of (3) has been represented in Fig. 2, for the initial filter design. An initial value of the VCO free-running frequency ω_o, close to the harmonic component $K_L = 162$, has been considered. As observed, the system phase-locks to $K_L = 163$. This is due to the duty cycle of the SPD output pulse, close to ½, which gives rise to spectral lines with theoretical zero value at even multiples of f_x.

Note that the phase-locked state is not given by a constant phase value $\phi = \phi_0$. The harmonic components of the pulse signal are still present in the solution, giving rise to the oscillating behavior about the constant frequency $f_L = 163\ f_x$. In phase-locked conditions, the VCO output frequency can be written:

$$f_o^v = U_o + M_1 \sum_k R_k e^{jkw_x t} = w_o + M_1 R_0 + M_2 \sum_{k\neq 0} R_k e^{jkw_x t} \qquad (4)$$

with R_k being the harmonic components of hyperbolic-tangent function, applied to the filter output. Note that:

$$K_L w_x = w_o + M_1 R_o \qquad (5)$$

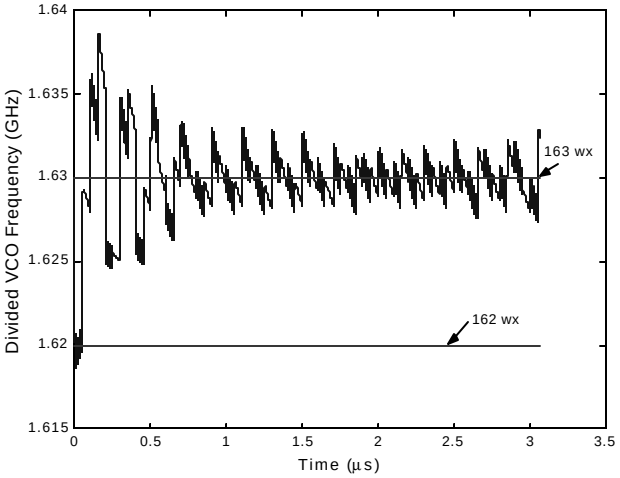


Fig. 2 Phase-locking of the SPD synthesizer to the harmonic component $K_L = 163$. The VCO free-running oscillator frequency is close to $\omega_o = 162\omega_x$

B. Phase-locked bands. Devil staircase

In order to determine the phase-locking bandwidth about each harmonic component $K_L f_x$, a bifurcation analysis has been carried out. Since the division order is kept constant at N = 4 and so is the reference frequency ω_x, the observation of phase locking will depend on the free-running value of the VCO frequency. This is the bifurcation parameter that has been considered here, applying the Poincaré-map technique [4]. In a non-autonomous system, as the one that is simulated here, this map is obtained by sampling the steady state solution at

integer multiples of the forcing-generator period (nT). This enables a dimension reduction of the system solution.

The application of the Poincaré map for successive values of ω_o (analysis parameter) provides the bifurcation diagram. The steady state is sampled at the time rate $T_s = 1/f_x$. The ratio f_o^n / w_x has been represented in Fig. 3a. Note that a straight line of constant-frequency value gives the phase-locking bandwidth about each harmonic component. It is not a perfect line, due to the oscillating term in (4). In the unlocked-behavior intervals, the solution is chaotic. The phase-locked bands, embedded within intervals of chaotic behavior, take the shape of a staircase, the resulting diagram being called *devil staircase* [4].

The diagram has been traced starting from $\omega_o/\omega_x = 160$ and moving rightwards. Close observation of each synchronization band, shows almost-continuous behavior on the left-side border and discontinuous behavior on the right-side one. The almost-continuous behavior indicates a *capture* phenomenon. From a nonlinear-dynamics point of view, this corresponds to the collision an unlocked solution of rotation type with a phase-locked solution of saddle type [2]. Both types of solutions are very close in the phase space when the collision happens, so the amplitude of the jump in the Poincaré map is small. The discontinuous behavior indicates the end of the *hold-in* range. This is due to a collision between the phase-locked solutions of saddle and node type and it is a discontinuous phenomenon, usually involving big-amplitude jumps, since, when it happens, the system solution jumps to the rotation that may be far in the phase space [2]. The occurrence of the two phenomena for different ω_o gives rise to hysteresis. The determination of the hysteresis ranges at both ends requires a new parameter sweep in the inverse sense, i. e., decreasing the ratio ω_o/ω_x. This has been traced in Fig. 3b, which shows the acquisition and hold-in bands about the harmonic of interest $K_L = 163$. The experimental determination of the phase-locking bands has been superimposed.

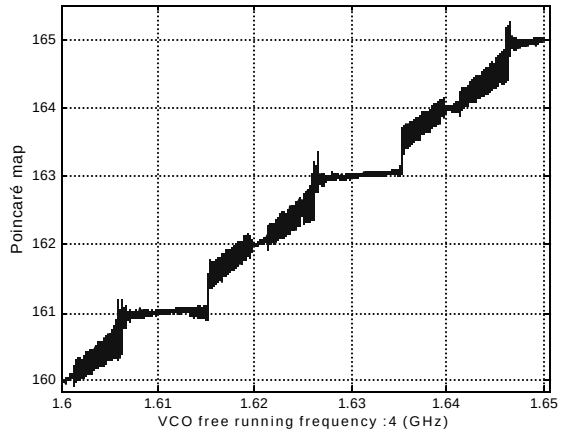
The observation of the devil staircase has been reported in electronic circuits, such as Chua's circuit, with a simple topology, (although complex behavior). To our knowledge, it is the first time that this bifurcation diagram is obtained in a phase-lock loop. The ranges with phase-locked behavior correspond to rational values of the rotation number, defined as the ratio between the two fundamental frequencies in the system:

$$r = \frac{w_x}{w_o + M_1 R_0} = \frac{1}{K_L} \qquad (6)$$

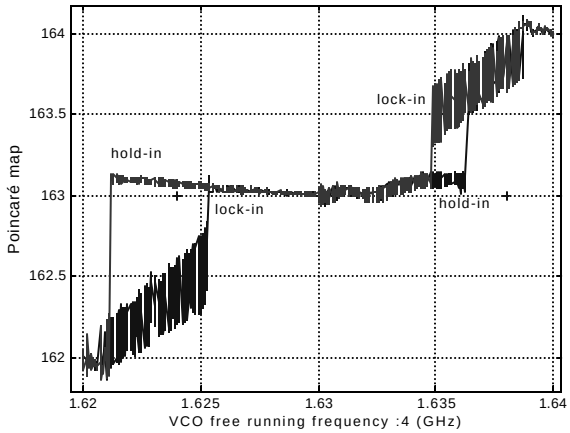
which is only valid in phase-locked behavior. The diagram in Fig. 3a is more complex than it appears, since embedded between the ranges of phase-locked behavior at $1/K_{L1}$ and $1/K_{L2}$, there are other synchronization bands with smaller bandwidth. These are obtained for rational numbers $r = 2/(K_{L+1}+K_{L+2})$. It has been shown that this bifurcation diagram has a fractal structure [4].

C. *Parametric analysis versus filter bandwidth*

The synthesizer is expected to operate in the phase-locked band corresponding to $K_L = 163$. Thus a second nonlinear analysis has been carried out to determine how the frequency interval of phase-locked behavior varies with the bandwidth of the loop-filter. This is shown in Fig. 4. The resulting diagram is the Arnold tongue [4], corresponding to the rotation number $r = 1/163$. The saturation effect is due to the influence of the neighboring harmonic components $K_L = 162$ and $K_L = 164$.



(a)



(b)

Fig. 3 Poincaré map of the SPD synthesizer. (a) *Devil staircase*. The nearly straight lines provide the acquisition bands about each K_L value. (b) Expanded-view about harmonic component K_L. Measurements superimposed.

D. Final design of the synthesizer and experimental results.

The linearization (1), used for the calculation of the phase noise, is only valid in case of restrictive filtering, when an almost-constant value of ϕ is obtained in (4). Otherwise the linearization has to be carried out about the actual steady state, with oscillating behavior. For the filter cut-off frequency f_c = 10 KHz, a substantial reduction of the time varying term of (4) is obtained, as shown in Fig. 5. This enables the use of the linear approximation (1) for the phase-noise prediction. Note that the nonlinear analysis of the system in the presence of noise fluctuations is very demanding from the computational point of view, due to the large bandwidth of the solution envelope (for a pulse-input signal). The phase-noise calculation gives the result L(10 KHz) = -81.17 dBc/Hz fulfilling the specification. The resulting experimental spectrum is shown in Fig. 6. According to Fig. 4 the phase-locking bandwidth is Δf_L = 85 KHz. Phase-locking without the use of acquisition aid has been possible.

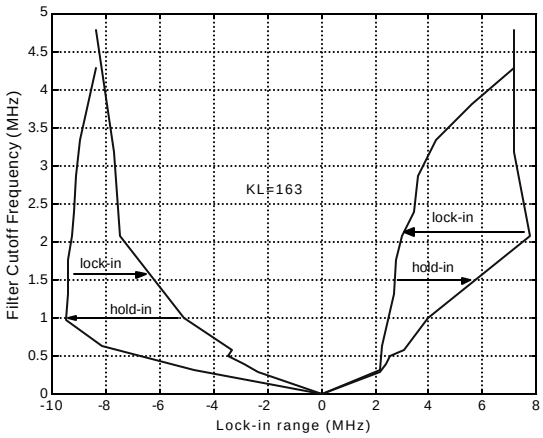


Fig. 4 Arnold tongue for K_L=163.

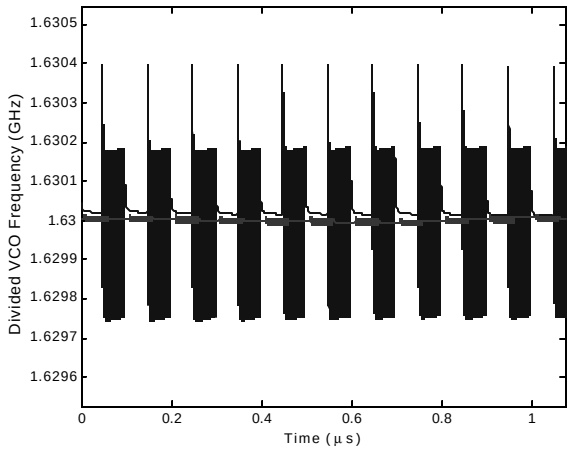


Fig. 5 Time variation of the VCO output frequency for two different values of the filter cut-off frequency. The higher amplitude variations correspond to f_c = 4.7 MHz and the lower ones to f_c = 300 KHz.

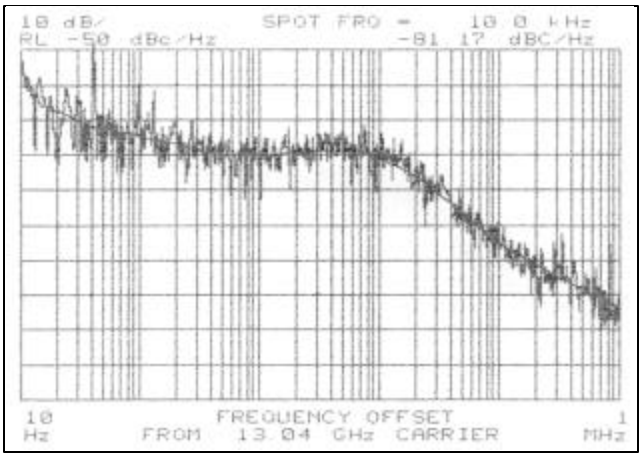


Fig. 6 Measured spectrum of the SPD synthesizer, after a frequency doubler.

IV. CONCLUSIONS

A microwave synthesizer, based on a sampling-phase detector, has been designed to satisfy a restricted phase-noise specification. The design has been carried out using nonlinear analysis tools, that have allowed a better understanding of the complex system dynamics. The use of the Poincaré-map technique has enabled the determination of the lock-in and hold-in bands about the desired harmonic component of the reference oscillator. A parametric analysis of these bands, versus the loop-filter cut-off frequency, has allowed an optimum loop-filter design to fulfill the phase-noise specification without a severe reduction of the system acquisition band.

REFERENCES

[1] J. Gismero, J. Grajal, "9 GHz phase locked oscillator using a sampling phase detector. Application to VSAT local oscillators (18-27 GHz)," *23th European Microwave Conference, Madrid*, pp. 784-786, October 1993.

[2] S. Sancho, A. Suárez, T. Fernandez, "Nonlinear analysis of microwave frequency synthesizers: stability and incidental FM," *2000 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 1, pp. 497-500, June 2000.

[3] L. Martin, "Program optimizes PLL phase-noise performance," *Microwaves and RF*, pp. 78-91, April 1992.

[4] T. Matsumoto, "Chaos in Electronic Circuits," *1987 IEEE Special Issue on Chaotic Systems*, vol. 75, no. 8, pp. 1033-1057, August 1987.